GROUP III NITRIDE WAFER AND ITS PRODUCTION METHOD

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. App. No. 61/694,119 filed Aug. 28, 2012, by inventors Tadao Hashimoto, Edward Letts, and Sierra Hoff, entitled "GROUP III NITRIDE WAFER AND ITS PRODUCTION METHOD", which is incorporated by reference in its entirety as if put forth in full below.

This application is related to the following U.S. patent applications:

PCT Utility Patent Application Serial No. US2005/024239, filed on Jul. 8, 2005, by Kenji Fujito, Tadao Hashimoto and Shuji Nakamura, entitled "METHOD FOR GROWING GROUP III-NITRIDE CRYSTALS IN SUPERCRITICAL AMMONIA USING AN AUTOCLAVE";

U.S. Utility patent application Ser. No. 11/784,339, filed on Apr. 6, 2007, by Tadao Hashimoto, Makoto Saito, and Shuji Nakamura, entitled "METHOD FOR GROWING LARGE SURFACE AREA GALLIUM NITRIDE CRYSTALS IN SUPERCRITICAL AMMONIA AND LARGE SURFACE AREA GALLIUM NITRIDE CRYSTALS," which application claims the benefit under 35 U.S.C. Section 119(e) of U.S. Provisional Patent Application Ser. No. 60/790,310, filed on Apr. 7, 2006, by Tadao Hashimoto, Makoto Saito, and Shuji Nakamura, entitled "METHOD FOR GROWING LARGE SURFACE AREA GALLIUM NITRIDE CRYSTALS IN SUPERCRITICAL AMMONIA AND LARGE SURFACE AREA GALLIUM NITRIDE CRYSTALS";

U.S. Utility Patent Application Ser. No. 60/973,662, filed on Sep. 19, 2007, by Tadao Hashimoto and Shuji Nakamura, entitled "GALLIUM NITRIDE BULK CRYSTALS AND THEIR GROWTH METHOD";

U.S. Utility patent application Ser. No. 11/977,661, filed on Oct. 25, 2007, by Tadao Hashimoto, entitled "METHOD FOR GROWING GROUP III-NITRIDE CRYSTALS IN A MIXTURE OF SUPERCRITICAL AMMONIA AND NITROGEN, AND GROUP III-NITRIDE CRYSTALS GROWN THEREBY";

U.S. Utility Patent Application Ser. No. 61/067,117, filed on Feb. 25, 2008, by Tadao Hashimoto, Edward Letts, Masanori Ikari, entitled "METHOD FOR PRODUCING GROUP III-NITRIDE WAFERS AND GROUP III-NITRIDE WAFERS";

U.S. Utility Patent Application Ser. No. 61/058,900, filed on Jun. 4, 2008, by Edward Letts, Tadao Hashimoto, Masanori Ikari, entitled "METHODS FOR PRODUCING IMPROVED CRYSTALLINITY GROUP III-NITRIDE CRYSTALS FROM INITIAL GROUP III-NITRIDE SEED BY AMMONOTHERMAL GROWTH";

U.S. Utility Patent Application Ser. No. 61/058,910, filed on Jun. 4, 2008, by Tadao Hashimoto, Edward Letts, Masanori Ikari, entitled "HIGH-PRESSURE VESSEL FOR GROWING GROUP III NITRIDE CRYSTALS AND METHOD OF GROWING GROUP III NITRIDE CRYSTALS USING HIGH-PRESSURE VESSEL AND GROUP III NITRIDE CRYSTAL";

U.S. Utility Patent Application Ser. No. 61/131,917, filed on Jun. 12, 2008, by Tadao Hashimoto, Masanori Ikari, Edward Letts, entitled "METHOD FOR TESTING III-NITRIDE WAFERS AND III-NITRIDE WAFERS WITH TEST DATA";

which applications are incorporated by reference herein in their entirety as if put forth in full below.

BACKGROUND

Field of the Invention

The invention is related to a semiconductor wafer used for various device fabrication including optoelectronic and electronic devices such as light emitting diodes, (LEDs), laser diodes (LDs), photo detectors, and transistors. More specifically, the invention is on a compound semiconductor wafer composed of group III nitride.

Description of the Existing Technology

(Note: This patent application refers several publications and patents as indicated with numbers within brackets, e.g., [x]. A list of these publications and patents can be found in the section entitled "References.")

Gallium nitride (GaN) and its related group III nitride alloys are the key material for various optoelectronic and electronic devices such as LEDs, LDs, microwave power transistors and solar-blind photo detectors. However, the majority of these devices are grown epitaxially on heterogeneous substrates (or wafers), such as sapphire and silicon carbide since GaN wafers are extremely expensive compared to these heteroepitaxial substrates. The heteroepitaxial growth of group III nitride causes highly defected or even cracked films, which hinder the realization of high-end electronic devices, such high-power microwave transistors.

To solve all fundamental problems caused by heteroepitaxy, it is indispensable to utilize group III nitride wafers sliced from group III nitride bulk crystals. For the majority of devices, GaN wafers are favorable because it is relatively easy to control the conductivity of the wafer and GaN wafer will provide the smallest lattice/thermal mismatch with most of device layers. However, due to the high melting point and high nitrogen vapor pressure at elevated temperature, it has been difficult to grow bulk GaN crystals. Currently, majority of commercially available GaN wafers are produced by a method called hydride vapor phase epitaxy (HVPE). HVPE is a vapor phase epitaxial film growth, thus difficult to produce bulk-shaped group III nitride crystals. Due to limitation of the crystal thickness, the typical density of line defects (e.g. dislocations) and grain boundaries is at the order of high 10^5 to low-10^6 cm^{-2}.

To obtain high-quality GaN wafers of which density of dislocations and/or grain boundaries is less than 10^6 cm^{-2}, a new method called ammonothermal growth has been developed [1-6]. Also, there are other bulk growth methods such as high-pressure solution growth or a flux method [7-10]. High-quality GaN wafers having density of dislocations and/or grain boundaries less than 10^6 cm^{-2} can be obtained by ammonothermal growth or other bulk growth methods. However, the utilization of a bulk growth method for wafer fabrication created a new problem which was not experienced when wafers were fabricated one by one with HVPE. In HVPE, thick film of group III nitride is epitaxially grown on a substrate such as sapphire or gallium arsenide. Then, the substrate is mechanically or chemically removed. In this way, one side of the group III nitride wafer is obviously distinguishable from the other side of the wafer because the top surface of an epitaxially grown film typically shows a crystallographic feature such as hillocks. On the contrary, wafer fabrication from bulk growth method typically involves slicing of wafers from grown bulk crystals. The bulk crystal is typically sliced into wafers with a multiple wire saw. Since the multiple wire saw is a mechanical means of cutting, the both surface of the sliced wafer become